The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CATHERINE B. LABELLE, BOON-YONG ANG,
JOONG S. JEON, ALLISON K. HOLBROOK,
QI XIANG, and HUICAI ZHONG

Appeal 2007-0287
Application 10/705,347
Technology Center 1700

Decided: March 16, 2007

Before BRADLEY R. GARRIS, THOMAS A. WALTZ, and
CATHERINE Q. TIMM, *Administrative Patent Judges.*

WALTZ, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on an appeal from the Primary Examiner's final rejection of claims 1, 6 through 8, 14 through 16, 19, and 20, which are the only claims pending in this application. We have jurisdiction pursuant to 35 U.S.C. §§ 6 and 134.

According to Appellants, the invention is directed to a method for forming a field-effect transistor on a substrate, where the substrate includes a high-k dielectric layer situated over the substrate, and a gate electrode layer situated over the high-k dielectric layer (Br. 3). The method includes the step of etching the gate electrode layer and the high-k dielectric layer in a plasma process chamber to form a gate stack, followed by a nitridation process using a nitrogen containing plasma in the plasma process chamber to nitridate the sidewalls and form an oxygen diffusion barrier (*id.*). Independent claim 1 is illustrative of the invention and is reproduced below:

1. A method for forming a field-effect transistor on a substrate, said substrate including a high-k dielectric layer situated over said substrate and a gate electrode layer situated over said high-k dielectric layer, said method comprising steps of:

etching said gate electrode layer and said high-k dielectric layer to form a gate stack, said gate stack comprising a high-k dielectric segment situated over said substrate and a gate electrode segment situated over said high-k dielectric segment;

performing a nitridation process on said gate stack, said nitridation process utilizing a nitrogen containing plasma to nitridate sidewalls of said gate stack, said nitridation process on said gate stack causing nitrogen to enter said high-k dielectric segment, said nitrogen forming an oxygen diffusion barrier in said high-k dielectric segment;

wherein said step of etching said gate electrode layer and said high-k dielectric layer to form said gate stack is performed in a plasma process chamber, said plasma process chamber being utilized to perform said step of performing said nitridation process on said gate stack.

The Examiner relies on the following references as evidence of obviousness:

Doyle	US 5,891,798	Apr. 06, 1999
Ballance	US 6,090,210	Jul. 18, 2000
Alers	US 6,265,260 B1	Jul. 24, 2001
Tu	US 6,566,250 B1	May 20, 2003
Aronowitz	US 6,759,337 B1	Jul. 06, 2004
Chang (Chang '240)	US 2004/0188240 A1	Sep. 30, 2004[1]
Chang (Chang '964)	US 2005/0019964 A1	Jan. 27, 2005
Colombo	US 2005/0079696 A1	Apr. 14, 2005

ISSUES ON APPEAL

Claims 1, 6-8, 14-16, 19, and 20 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Colombo or Doyle in view of Alers or Tu, further "as evidenced" by Chang '240, Ballance, Aronowitz, or Chang '964 (Answer 3 and 4).[2]

Appellants contend that Colombo does not disclose, teach, or suggest utilizing a plasma, much less using the same plasma chamber for both the gate etch and nitridation processes (Br. 8).

Appellants contend that Doyle does not suggest that the processes of etching the gate stack and the nitridation of the etched gate stack are performed in a single plasma chamber (Br. 12).

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[1] We note that Chang '240 is mistakenly omitted in the "Evidence Relied Upon," with Chang '964 cited two times (Answer 2-3, ¶ (8)). However, we deem this error harmless since the references are correctly listed both in the Brief (page 6) and the statement of the rejection in the Answer (page 3).

[2] For purposes of judicial economy, we list the two separate rejections in the Answer as one rejection with alternate primary references, since both rejections on appeal include the same claims with the same secondary references applied for the same reasons (Br. 6; Answer 3 and 4).

Appellants further contend that the secondary references to Alers, Tu, Chang '240, Ballance, Aronowitz, and Chang '964 do not suggest application of their disclosures to plasma nitridation of gate stacks in transistors after a gate etch (Br. 8-10 and 12).

The Examiner contends that both Colombo and Doyle teach the benefits of nitridation in the presently claimed process, and that Alers and Tu show that it was conventional in the art to nitridate with a nitrogen plasma (Answer 3-6).

The Examiner contends that Chang '240, Ballance, Aronowitz, and Chang '964 are "evidence to show that 'performing both etching and nitridation in the same plasma process chamber' is ... well known in the art of semiconductor device fabrication." (Answer 6).

Accordingly, the issues presented in this appeal are as follows: (1) was it well known in this art to use a plasma containing nitrogen as a means for effecting nitridation? and (2) was it well known in this art to perform both etching and nitridation in the same plasma process chamber?

We determine that the Examiner has established a prima facie case of obviousness in view of the reference evidence. We also determine, based on the totality of the record, including due consideration of Appellants' arguments, that the preponderance of evidence weighs most heavily in favor of obviousness within the meaning of § 103(a). Therefore we AFFIRM all grounds of rejection in this appeal essentially for the reasons stated in the Answer, as well as those reasons stated below.

OPINION

We determine the following factual findings from the record in this appeal:

(1) Colombo and Doyle disclose methods for forming a field-effect transistor on a substrate, including placing a high-k dielectric layer over the substrate, a gate electrode layer over the high-k dielectric layer, and etching both layers to form a gate stack (Answer 3-4);[3]

(2) Colombo and Doyle both teach the benefits of performing a nitridation process on the gate stack, i.e., to avoid oxidation of the gate stack layers and facilitate repairing of these layers (Colombo, ¶ [0022]), or to prevent oxidation at the upper interface of the gate dielectric (Doyle, col. 5, ll. 6-9);

(3) Colombo teaches that nitridation may be accomplished by any suitable technique (¶ [0011]) and Doyle teaching nitridation by implanting nitrogen into the polysilicon gate electrode (col. 4, l. 63-col. 5, l. 6);

(4) Colombo suggests that the nitridation can be accomplished by "plasma nitridation" such as decoupled-plasma-nitridation (DPN) (page 2, claim 8, and ¶ [0011]);

(5) Colombo teaches that nitriding the sidewalls of a patterned gate structure, and forming a silicon nitride encapsulation layer along the sidewalls can be performed in sequence in a single processing chamber (¶ [0011]);

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[3] Appellants admit that this part of the claimed process is "a conventional transistor fabrication process" (Specification 1:17 – 2:2).

(6) Alers teaches that using a nitrogen containing plasma for nitridation is a conventional technique in the semiconductor art (col. 3, ll. 40-44);

(7) Tu teaches that "a conventional nitridation step is carried out by exposing the metal to a nitrogen containing plasma" (col. 6, ll. 7-11);

(8) Chang '240, Ballance, Aronowitz, and Chang '964 all teach or exemplify a single processing chamber used in sequence for two processes, e.g., etching followed by plasma deposition (Chang '240, ¶ [0040]; Ballance, col. 1, ll. 31-34; Aronowitz, col. 2, ll. 45-50, and Chang '964, ¶ [0041]).

The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art. *See In re Young,* 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991); *In re Keller,* 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). It is well established that before a conclusion of obviousness may be made based on a combination of references, there must have been a reason, suggestion, or motivation to lead an inventor to combine these references. *See Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.,* 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1629 (Fed. Cir. 1996).

Applying these legal principles to the factual findings on this record in this appeal, we determine that the Examiner has established a prima facie case of obviousness in view of the reference evidence. We also determine that Appellants have not adequately rebutted this prima facie case of obviousness by their arguments. As established by the factual findings listed

above, Colombo not only teaches the etching process and the benefits of the nitridation process, but further teaches using a plasma to effectuate the nitridation (factual finding (4) above). Furthermore, Colombo teaches that nitridation can be accomplished by "any suitable technique" (factual finding (3) above). Alers and Tu both teach "conventional techniques" for nitridation involving the use of a nitrogen plasma (factual findings (6) and (7) above). We determine that this teaching by Colombo would have suggested or motivated one of ordinary skill in this art to use conventional techniques such as those disclosed by Alers and Tu. We further determine that the Examiner has established that it was well known in the art to use a single processing chamber for two or more process steps. *See* factual finding (5) above, where Colombo suggests using the same process chamber for two process steps. *See* also factual finding (8) above, where the Examiner cites four references to establish that it was well known in the semiconductor fabrication art to perform etching and plasma deposition steps in the same processing chamber. We determine that the Examiner has set forth sufficient reasoning to use a single processing chamber, namely that such a step is "efficient and more cost effective" (Answer 4-6). Appellants have not disputed this reasoning (see the Brief in its entirety).

For the foregoing reasons and those stated in the Answer, we affirm both rejections on appeal. The decision of the Examiner is thus affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2006).

AFFIRMED

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